MASTER DRAWING LIST

MAINTENANCE MANUALS NO.	TITLE	UNIT VARIATIONS DP8-EA	DP8-EB
DP8-E	SYNCHRONOUS MODEM INTERFACE	X	X

USED ON OPTIONS							
PDP8-E							
PDP8M							
PDP8F							

REVISIONS REV.	DATE	CHG. NO.	APP'D.
A	3-72	DP8E-00001	
B	4-72	M839-0002A	
C	7-72	DP8E-00002	
D	10/72	DP8E-00003	

DRN. R. SMITH DATE 6/17/71
CHK'D. K. GULICK DATE 6/17/71
ENG. DATE
PROJ. ENG. DATE
PROD. R.K. Allen DATE 7-2-71
FIRST USED ON PDP8-E
SCALE NONE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNCHRONOUS MODEM INTERFACE

SIZE	CODE	NUMBER	REV.
A	ML	DP8-E	D

DIST.

DRA 131

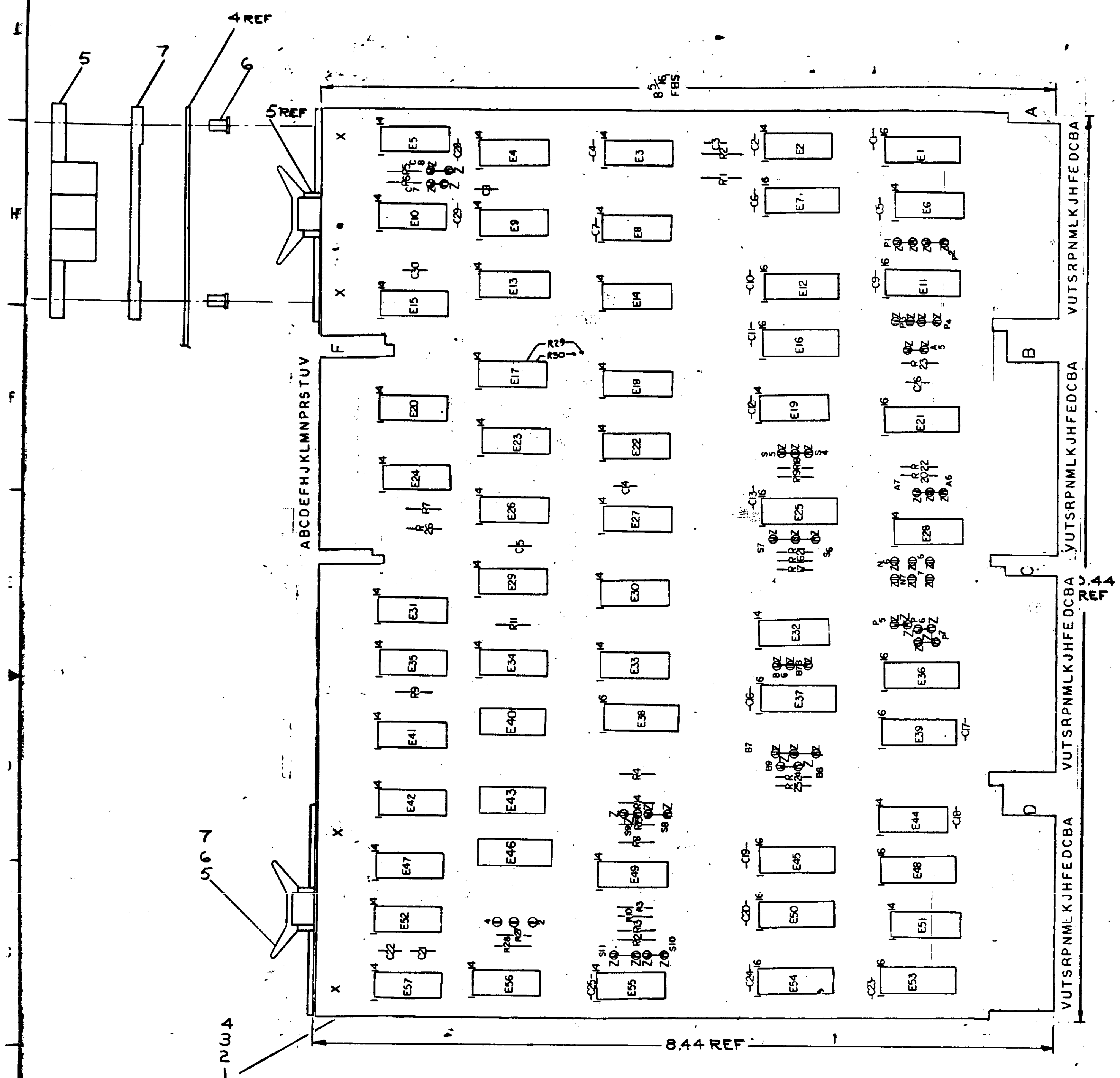
PRINT SET DP8-E	DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE	OPTION NO.
X	E-CS-M839-Ø-1	#	2	SYNCHRONOUS MODEM INTERFACE	
X	E-CS-M866-Ø-1	#	2	SYNCHRONOUS MODEM INTERFACE	
X	D-UA-BCØ1W-25-Ø	#	1	BCØ1W CABLE ASSY	
X	A-SP-DP8-E-1	C	32	ENGINEERING SPECIFICATIONS	
-	A-SP-DP8-E-2	B	14	TEST PROCEDURE	
-	A-SP-DP8-E-3	B	10	ACCEPTANCE PROCEDURE DP8-EA	
X	D-AD-7008372-0-0	#	1	TEST CONNECTOR	DP11
X	D-UA-BCØ5C-0-0	#	1	BCØ5C CABLE ASSY	
-	A-SP-DP8-E-5		8	ACCEPTANCE PROCEDURE DP8-EB	
-					
-	LIBKIT-8E-DP8A	#	REF	SOFTWARE KIT LIST	
X	A-PL-DP8-E-0		1	PARTS LIST	
X	A-AL-DP8-E-4		1	DP8-E ACCESSORY LIST	

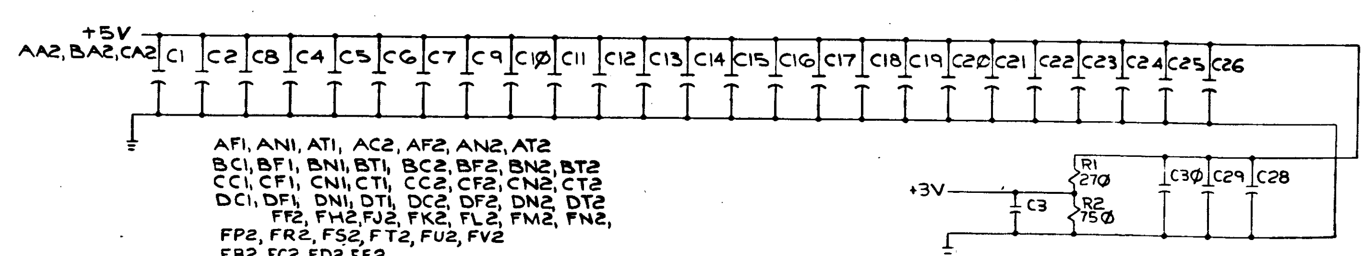
TITLE SYNCHRONOUS MODEM INTERFACE

SHEET 2 OF 2

SIZE	CODE	NUMBER	REV.
A	ML	DP8-E	D

DRA 132





NOTES:

1. UNLESS OTHERWISE NOTED:
CAPACITORS ARE .01μF 100V 20%
RESISTORS ARE 3K 1/4W 5%.

2. JUMPER SELECTION

SELECT			REMOVE JUMPER (ASSUMING ALL JUMPERS ARE IN)
BITS/CHAR-ACTER	6		B8, B7, B78, C7, B9
	7		B8, B6, C8, B9
	8		B7, B6 C7
BREAK PRIORITY	1-7		REMOVE P1-P7 EXCEPT FOR "P" NUMBER CORRESPONDING TO REQUIRED PRIORITY.
ACCESS ADDRESS	7720	1ST DP8	A6
	7700	2ND "	A6, A7
	7660	3RD "	A5
	7640	4TH "	A5, A7
	7620	SPARE	A5, A6
	7600	SPARE	A5, A6, A7
DEVICE CODE	640X/641X	1ST DP8	5, 6, 7
	642X/643X	2ND "	5, 6, N7
	644X/645X	3RD "	5, N6, 7
	646X/647X	4TH "	5, N6, N7
	630X/631X		N5, 6, 7
	632X/633X		N5, 6, N7
	634X/635X		N5, N6, 7
	636X/637X		N5, N6, N7
SYNC CODE	226		S5, S6, S8, S11
	ZERO		S4-S11
CHARACTER RECOGNITION	NR OF CHAR		NEVER RUN THE DP8E WITH BOTH 2 & 4 REMOVED. THIS WILL CAUSE NO RECEIVE WC CYCLE.
	4 CHAR		NONE
	2 CHAR		2
	0 CHAR		4

QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E23	I.C. DEC 74H74	1909667	34
57		SPLIT LUGS	9006735	33
A/R		WIRE #22 AWG SOLID BUS	9107560-01	32
3	E5, 10, 52	IC DEC 74197	1910035	31
1	E24	IC DEC 74H10	1909057	30
1	E44	IC DEC 74H04	1909931	29
2	E26, 31	IC DEC 74H00	1909056	28
6	E1, 21, 36, 48, 53, 11	IC DEC 8235	1909935	27
2	E25, 45	IC DEC 8266	1909934	26
2	E32, 55	IC DEC 8242	1909712	25
3	E22, 33, 34	IC DEC 8881	1909705	24
1	E19	IC DEC 314	1909704	23
1	E40	IC DEC 7404	1909686	22
7	E7, 12, 16, 37, 39, 50, 54	IC DEC 8271	1909615	21
2	E38, 46	IC DEC 8251	1909594	20
3	E17, 35, 49	IC DEC 384	1909486	19
4	E6, 14, 28, 51	IC DEC 380	1909485	18
4	E4, 20, 30, 56	IC DEC 7402	1909004	17
1	E43	IC DEC 7420	1905577	16
2	E3, 42	IC DEC 7410	1905576	15
4	E8, E13, E18, E47	IC DEC 7400	1905575	14
7	E2, 9, 15, 27, 29, 41, 57	IC DEC 7474	1905547	13
1	R1	RESISTOR-270Ω, 1/4W, 5% CC	1301972	12
2	R2, R21	RESISTOR-750Ω, 1/4W, 5% CC	1301401	11
17	R5, 6, 12-20, 22-25, 27, 28	RESISTOR-3K, 1/4W, 5% CC	1300432	10
10	R3, R4, R7-R11, R26, R29, R30	RESISTOR-1K, 1/4W, 5% CC	1300365	9
29	C1-C26, C28-C30	CAP. .01μf 100V. 20% DISC.	1001610	8
2		SPACER (CABLE CLAMP)	1202704	7
4		EYELET GS4-11 STIMPSON	9006750	6
2		HANDLE FLIP CHIP-MAGENTA	9008337-6	5
1		ETCHED CIRCUIT BOARD	5009505	4
REF		MODULE HISTORY LIST	B-MH-M839-0-6	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M839-0-5	2
REF		X-Y COORDINATE HOLE LOC.	K-CO-M839-0-4	1

PARTS LIST

ETCH BOARD REV L

IC TYPE	GND	+5V
DEC 314	1	8
DEC 8271	8	16
DEC 8251	8	16
DEC 384	1	8
DEC 380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTFULLY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO	AWG	FROM PT	TO PT
32	22	SEE NOTE 2	

JUMPER LIST

DEC NO.	EIA NO.	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

DIGITAL EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

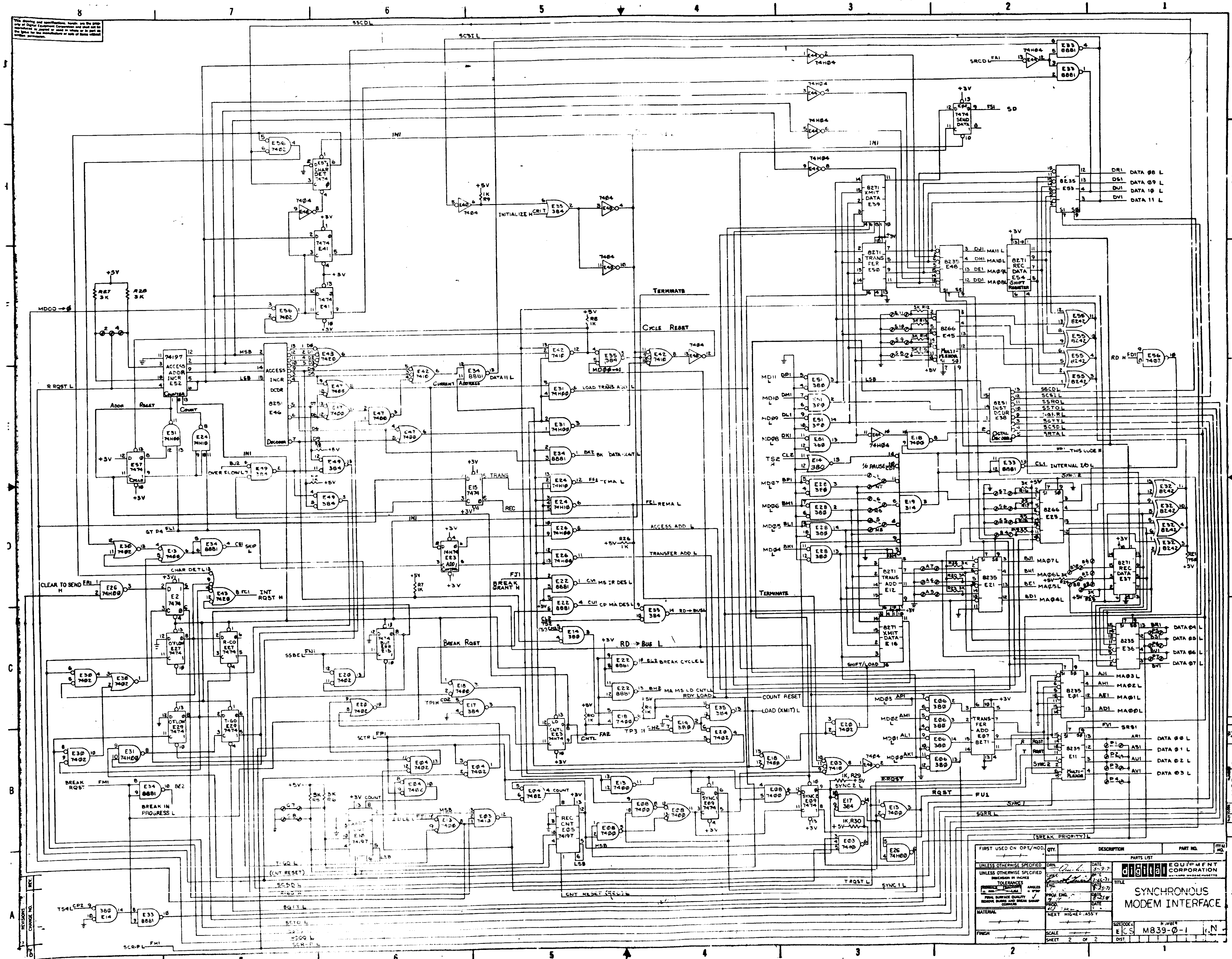
TITLE: SYNCHRONOUS MODEM INTERFACE

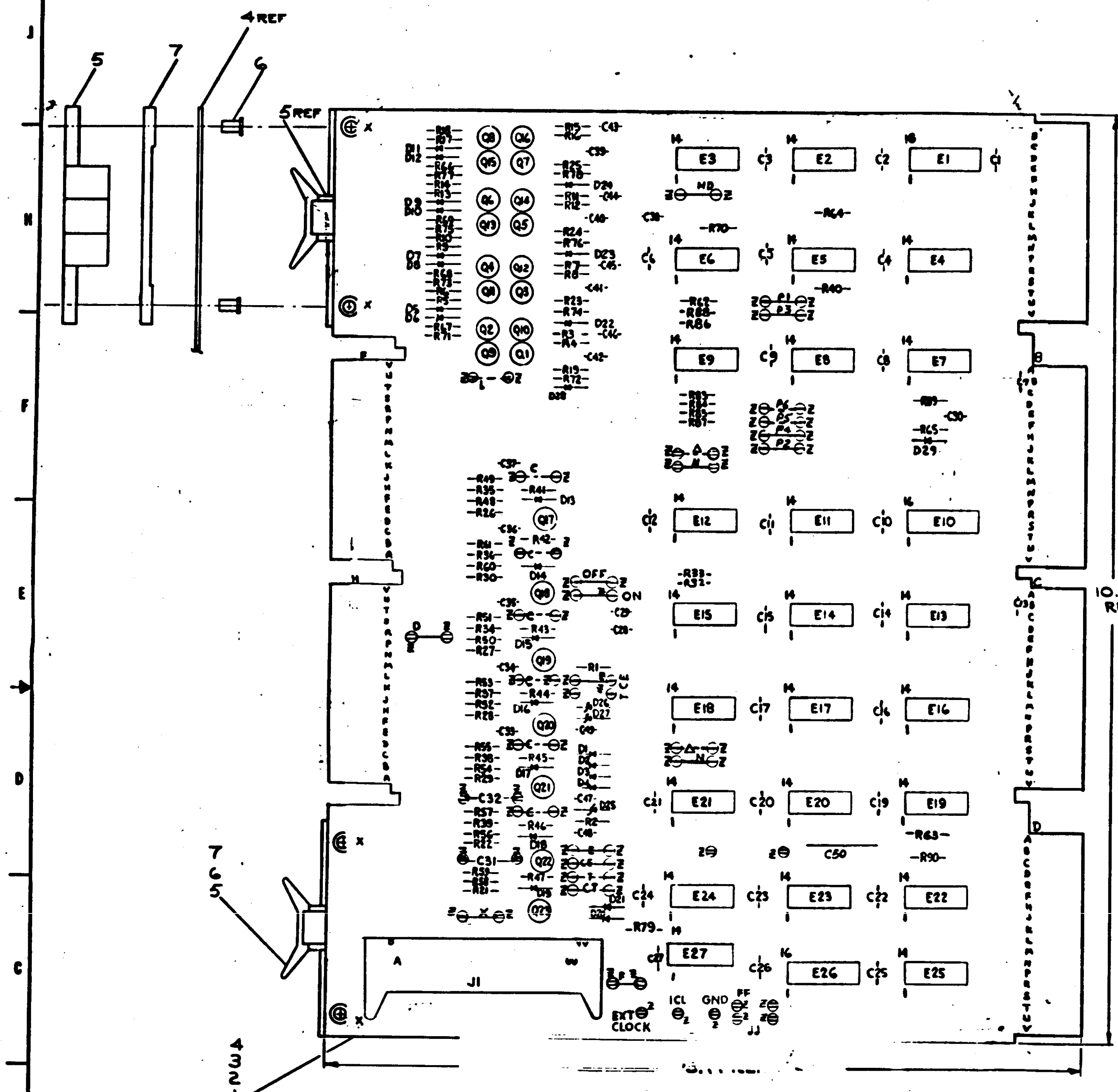
FIRST USED ON: A-ML-DP8-EA

SCALE 2/1 — SHEET 1 OF 2

SIZE E — CODE CS — NUMBER M839-0-1 — REV. N

DEC FORM NO. DWG 100


digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
SYNCHRONOUS MODEM INTERFACE
SIZE E
CODE CS
NUMBER M839-Ø-1
REV N
SHEET 2 OF 2
FIRST USED ON OPT./MOD.
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
ANGLES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D
ENG.
PROJ. ENG.
PROD.
NEXT HIGHER ASS'Y
SCALE
DIST.



NOTES:

1. UNLESS OTHER NOTED:
   RES. ARE 820 1/4W 5%
   CAP. ARE .01μf 100V 20%
   DIODES ARE 1/4 M 2A RZ
2. JUMPERS ARE:
   C = CURRENT MODE — HD = HALF DUPLEX
   E = EIA/CCITT — T = TTL
   N = NORMAL — Δ = INVERTED
3. ⊕ INDICATES SPLIT LUGS
4. SCT-P ≈ 50NS
5. SCR-P ≈ 100NS
6. TTL INPUT: CHANGE CAP TO 100 PF
7. TEST CONNECTOR:

SEND	REC
RS	CS & DATA SET RDY
SD	RD
TERM RDY	CO & RING (DELAYED DUE TO FILTER)
EXT TIMING	SCR & SCT

8. LEVEL CONVERSION:

TRANSMIT

TTL AT DIODE	CONVERTED OUTPUT EIA	CURRENT MODE	TTL
+3	-6	-0.7	-0.7
0V	+6.4	+6.4	+3.9

RECEIVE

EIA/TTL/CURRENT MODE	CONVERTED INPUT (TTL)
>1.5	3 < VOLTS < 5
<1.5	0 VOLTS

9. JUMPER SELECTION: JUMPERS ARE PRODUCTION INSERTED WITH THE EXCEPTION OF C & Δ

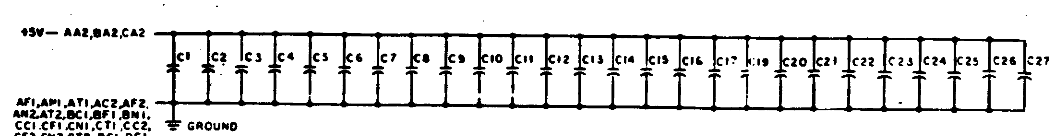
	SELECT	ACTION	JUMPER
CO/AGC TRANSITION	ON	REMOVE	OFF
	OFF	REMOVE	ON
	NONE	REMOVE	ON & OFF
CLOCK PHASE INVERTED		REMOVE	N
		ADD	Δ
LEVEL CONVERSION	EIA	REMOVE	T, CT
	CURRENT	REMOVE	E, T
	CURRENT	ADD	C
	TTL	REMOVE	E, CE
BREAK PRIORITY (DETECT)	1	REMOVE	P1-P6
	2		P2-P6
	3		P3-P6
	4		P4-P6
	5		P5-P6
	6		P6-
	7	REMOVE	—
MODEM SELECTION (CURRENT MODE)	BELL 201	REMOVE	D, X
	BELL 303	ADD	D, X

10. ICL JUMPER SELECTS INTERNAL RC CLOCK TO USE SPARE TRANSMITTER. TO PIN 11 WITH F JUMPER INSTALLED; TO PIN 24 WITH L JUMPER INSTALLED.

11. CAP ALLOWS USER TO INCREASE/DECREASE CLOCK SPEED: T = .87 (C·220)

QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	C50	CAP .047μf 100V 10%	1000051	46
1	J1	40 PIN CONNECTOR	1209941	45
1	R65	RES. 750, 1/4W, 5%	1301401	44
1	R89	RES 1K, 1/4W, 5%	1300365	43
71		SPLIT LUGS	9006735	42
A/R		WIRE #22 AWG SOLID BUS	9107560-01	41
3	E2, E11, E14	IC DEC 74197	1910035	40
1	E13	IC DEC 74H11	1909267	39
1	E16	IC DEC 74H74	1909667	38
3	E15, E20, E23	IC DEC 7402	1909004	37
2	E1, E10	IC DEC 8235	1909935	36
1	E9	IC DEC 7430	1905578	35
1	E26	IC DEC 8251	1909594	34
3	E7, E22, E25	IC DEC 380	1909485	33
1	E6	IC DEC 9601	1909373	32
2	E4, E19	IC DEC 8881	1909705	31
1	E5	IC DEC 384	1909486	30
3	E3, E24, E27	IC DEC 7474	1905597	29
2	E18, E17	IC DEC 7400	1905575	28
3	E12, E21, E8	IC DEC 7404	1909686	27
2	D26, D27	DIODE 1/4M 2.4 AZ	1101938	26
1	D25	DIODE 1N750A 1/4W 4.7V	1100124	25
22	D5 THRU D24, D28, D29	DIODE D664	1100114	24
4	D1 THRU D4	DIODE D662	1100113	23
15	Q9 THRU Q23	TRANSISTOR DEC 3009B	1503100	22
8	Q1 THRU Q8	TRANSISTOR DEC 6534C	1503404-02	21
3	C28, C29, C30	CAP 330 PF 100V 5% DM	000023	20
33	C1-C17, C19-C27, C43-C49	CAP .01μf 100V 20% DISC	001610	19
2	C33, 34	CAP 180PF	[illegible]	18
10	C31, C32, C35-C42	CAP 100 PF 100V 5% DM	1000016	17
13	R48 THRU R62	RES 1.5K 1/4W 5% CC	1300391	16
4	R66 THRU R69	RES 390 1/4W 5% CC	1300309	15
2	R63, R64	RES 470 1/4W 5% CC	1300316	14
17	R19, R21-R30, R43-R48	RES 2.7K 1/4W 5% CC	1300426	13
3	R32, R33, R40	RES 220 1/4W 5% CC	1300271	12
19	R1 THRU R18, R79	RES 820 1/4W 5% CC	1301775	11
6	R34 THRU R39	RES 100 1/4W 5% CC	1300229	10
9	R70 THRU R78	RES 7.5K 1/4W 5% CC	1301422	9
8	R40 THRU R47	RES 4.7K 1/4W 5% CC	1300397	8
2		SPACER (CABLE CLAMP)	1202704	7
4		EYELET GS4-11 STIMPSON	9006750	6
2		HANDLE FLIP CHIP-MAGENTA	9008106	5
1		ETCHED CIRCUIT BOARD	5009106	4
REF		MODULE HISTORY LIST	B-MH-M966-0-6	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M966-0-5	2
REF		X-Y COORDINATE HOLE LOC.	K-CO-M966-0-4	1

PARTS LIST



AF1, AP1, AT1, AC2, AF2, AN2, AT2, BC1, BF1, BN1, CC1, CF1, CN1, CT1, CC2, CF2, CN2, CT2, DC1, DF1, DN1, DT1, DC2, DF2, DN2, DT2, FA2, FB2, FC2, FD2, FE2, FF2, FH2, FJ2, FK2, FL2, FM2, FN2, FP2, FR2, FS2, FT2, FU2, FV2, BT1, BC2, BF2, BN2, BT2, HT1, J1A, J1B, J1C, J1D, J1E, J1H, J1K, J1M, J1P, J1S, J1U, J1W, J1Y, J1AA, J1CC, J1EE, J1HH, J1KK, J1MM, J1PP, J1SS, J1UU, J1VV.

IC TYPE	GND	+5V
DEC 8251	8	16
DEC 380	1	8
DEC 384	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO	AWG	FROM PT	TO PT
41	SEE NOTE #9		
41			

JUMPER LIST

FIRST USED ON OPT/MOD: DP8-EA

ETCH BOARD REV: M

DEC NO.	EIA NO
6534C	NONE
1N750A	SAME
3009B	2N3646
MM 2ARZ	1N4370
D664	1N3606
D662	1N645

SEMICONDUCTOR CONVERSION CHART

EQUIPMENT CORPORATION

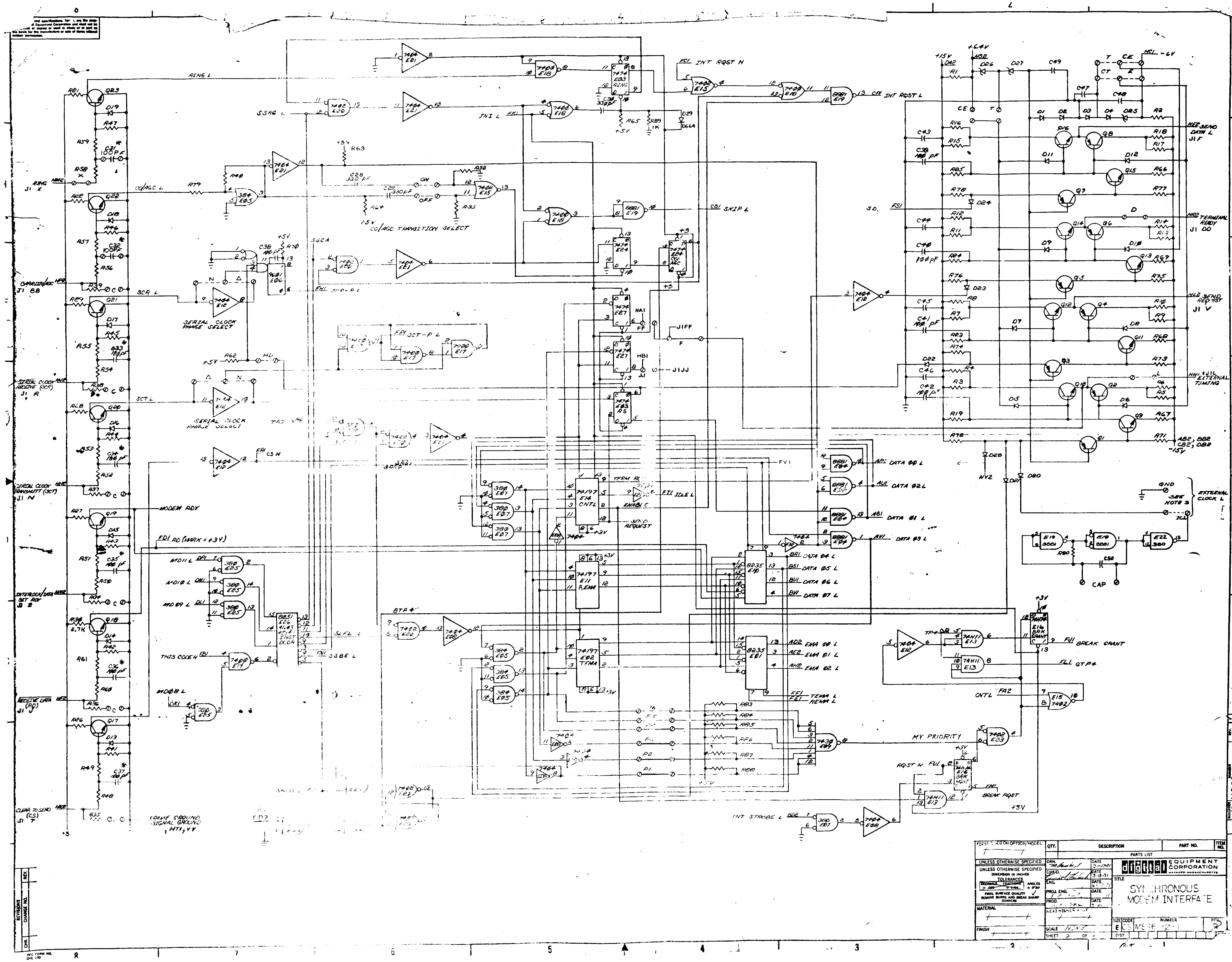
TITLE: SYNCHRONOUS MODEM INTERFACE

A ML-DP8-EA

SIZE: E — CODE: CS — NUMBER: M966-0-1 — REV. R

SCALE 2/1 — SHEET 1 OF 2

REVISIONS: E — ORIGINATED — M966-0001 — SMITH



RING L
SSNG L
INT RQST H
INT RQST L
CO/AGC L
CO/AGC TRANSITION SELECT
SKIP L
SCR L
SERIAL CLOCK PHASE SELECT
SCT L
CS H
MODEM RDY
RD (MARK = +3V)
THIS CODE H
SEND DATA L
TERMINAL READY
SEND REQUEST
EXTERNAL TIMING
EXTERNAL CLOCK L
DATA Ø0 L
DATA Ø1 L
DATA Ø2 L
DATA Ø3 L
DATA Ø4 L
DATA Ø5 L
DATA Ø6 L
DATA Ø7 L
EMA Ø0 L
EMA Ø1 L
EMA Ø2 L
TEMA L
REMA L
BREAK GRANT
MY PRIORITY
BREAK RQST
INT STROBE L
FRAME GROUND
SIGNAL GROUND
CAP
SYNCHRONOUS MODEM INTERFACE
DIGITAL EQUIPMENT CORPORATION
CS M866-0-1

FUNCTION	WIRE	CONNECTION FROM	CONNECTION TO
CLEAR TO SEND (CS)	C COND	P1 — C	J1 — T
SEND REQUEST (SR)	D COND	P1 — D	J1 — V
SEND DATA (SD)	E COND	P1 — E	J1 — F
DATA SET READY (DSR)	F COND	P1 — F	J1 — Z
RING INDICATOR (RI)	F SHIELD	P1 — F	J1 — X
LOCAL TEST (LT)	G COND	P1 — G	J1 — FF
SERIAL CLOCK TRANSMIT (SCTE)	H COND	P1 — H	J1 — L
SERIAL CLOCK TRANSMIT (SCT)	J COND	P1 — J	J1 — N
RECEIVE DATA (RD)	K COND	P1 — K	J1 — J
SERIAL CLOCK RECEIVE (SCR)	L COND	P1 — L	J1 — R
AGC LOCK (AGC)	M COND	P1 — M	J1 — BB
DATA TERMINAL READY (DTR)	M SHIELD	P1 — M	J1 — DD
	C SHIELD	P1 — C	J1 — A
	D SHIELD	P1 — D	J1 — A
	E SHIELD	P1 — E	J1 — B
	G SHIELD	P1 — G	J1 — B
	H SHIELD	P1 — H	J1 — VV
	J SHIELD	P1 — J	J1 — VV
	K SHIELD	P1 — K	J1 — UU
	L SHIELD	P1 — L	J1 — UU
	A	P1 — A	NC
	B	P1 — B	NC

WIRE REFERENCE TABLE	
A	LOCATION
TRACER	OF
G	WIRES
B	IN
H	WOVEN
C	CABLE
J	
D	
K	
E	
L	
F	
M	

NOTES:

A. A TWISTED PAIR WIRE (INCLUDING WILL BE ATTACHED TO EACH CONDUCTOR OF EACH WIRE (1 WIRE TO INNER CONDUCTOR, 1 WIRE TO THE SHIELD). THE WIRES WILL THEN BE CRIMPED TO THE BERG PINS AS INDICATED.

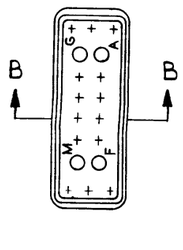
B. WHEN SUPPLIED BY A VENDOR THIS CABLE WILL BE FULLY TESTED BY VENDOR. TESTED AND INSPECTED BY INCOMING INSPECTION PRIOR TO ACCEPTANCE.

C. THIS IS THE CABLE DESCRIBED BY PURCHASE SPECIFICATION 17-00019.

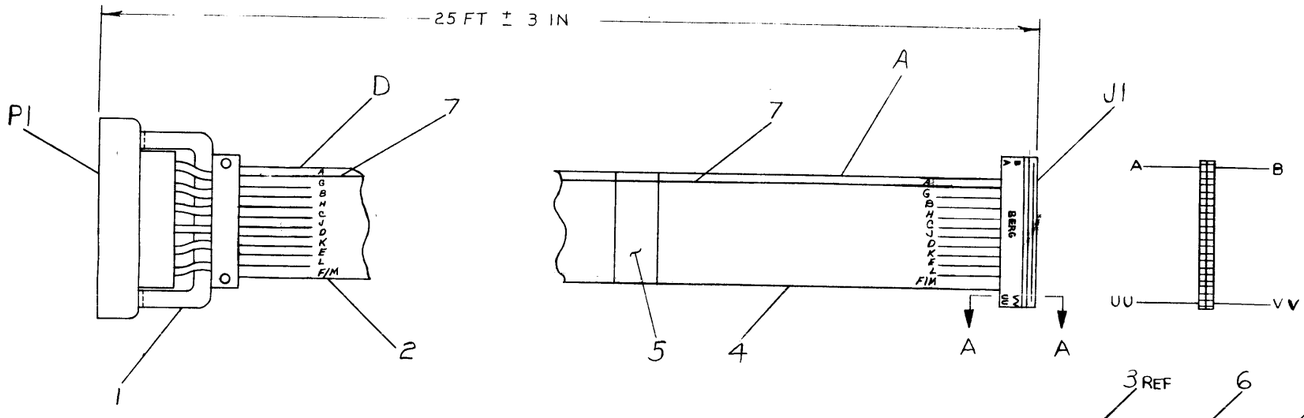
D. A COLORED TRACER WILL BE WOVEN INTO THE CABLE BETWEEN WIRES 'A' AND 'G'.

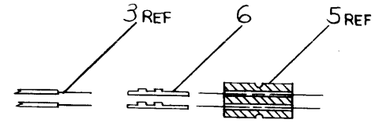
E. RG195 A/U CAN BE USED TO DIRECTLY REPLACE RG 180U.

F. NO SUBSTITUTIONS, OTHER THAN THOSE SPECIFIED IN THIS PRINT, MAY BE MADE WITHOUT PRIOR APPROVAL.



SECTION B-B





SECTION A-A

REV	CHANGE NO.	CHK	
A	BC01W-00001	DM	Implemented 2-12-72 SMITH 7-14-72

ITEM NO.	QTY.	DESCRIPTION	PART NO.
7	A/R	COLORED TRACER	
6	A/R	BERG PINS	12-10087-
5	A/R	INSULATION	
4	A/R	WIRE 26/28 AWG TWP	
3	1	CONN BERG	12-10090-00
2	A/R	CABLE COAX RG180 B/U	
1	1	BURNDY M012 MXP-17TC	

PARTS LIST

FIRST USED ON OPTION/MODEL

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005	±0° 30'
XX = .02	
X = .1	

REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓

MATERIAL

FINISH

		DATE
DRN	[illegible]	2-1-72
DES	[illegible]	8-23-72
ENG	[illegible]	3-23-72
PROJ. ENG	[illegible]	3-23-72
PROD.	[illegible]	3-24-72

NEXT HIGHER ASSY.

SCALE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: HIGH SPEED MODEM CABLE

SIZE	CODE	NUMBER	REV.
D	UA	BC01W-0-0	A

DIST.

DEC FORM NO DRD 100-A

SIZE D CODE UA NUMBER BC01W-0-0 REV A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 1 July 71

TITLE SYNCHRONOUS MODEM INTERFACE DP8-EA/EB

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		M839-0002A	B.SMITH	4/72		4-72
B	ECO CHANGE	DP8E-00002	B. SMITH	7/72		7-72
C	ECO CHANGE	DP8E-00003	B. SMITH	10/72		11-72

ENG	APPD	SIZE	CODE	NUMBER	REV
R. M. SMITH	2-18-72	A	SP	DP8-E-1	C

DEC FORM NO. DRA 107

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE SYNCHRONOUS MODEM INTERFACE - DP8-EA/EB

TABLE OF CONTENTS

1.0 DESCRIPTION

2.0 SPECIFICATIONS

- 2.1 Modem Interface
- 2.2 Transfer Mode
- 2.3 Character Parameters
  - 2.3.1 Bits Per Character
  - 2.3.2 Baud Rate
- 2.4 Data Transfers
- 2.5 Control Transfers
- 2.6 Clocks
- 2.7 Device Codes
- 2.8 Options
- 2.9 Cycle Time
- 2.10 Response
  - 2.10.1 Data Transfers
  - 2.10.2 Program Interrupts
- 2.11 Break Priority
- 2.12 Character Recognition
- 2.13 Power Consumption
  - 2.13.1 M839
  - 2.13.2 M866
- 2.14 Access Address
- 2.15 Synchronizing Character
- 2.16 Modem Compatability (Typical)
- 2.17 Carrier Detection

3.0 PROGRAMMING

- 3.1 Bit Assignments and/or Description

SIZE	CODE	NUMBER	REV
A	SP	DP8-E-1	C

DEC FORM NO 16-1022

3.1.1 Status
3.1.2 Access Address
3.1.3 Word Count and Current Address
3.1.4 Transmit and Receive Data
3.1.5 Control Word
3.1.6 Character Recognition
3.1.7 Field Selection
3.1.8 Character Detected (SRCD)

3.2 Instructions

3.2.1 Detailed
3.2.2 Summary

4.0 MISCELLANEOUS

4.1 Test Procedure
4.2 DP8-E Terminated Modem Leads (301, 303, 201)
4.3 DP8-E Assembly
4.4 Jumper Selection
4.5 Flow Charts

4.5.1 DP8-E Break Cycle
4.5.2 Programming

4.6 Top Connectors and I/O Pin Assignments

APPENDIX

A. RS232C Electrical Specifications
B. Current Mode Electrical Specifications
C. RS232C Interface Pin Assignments
D. RS232C to CCITT Equivalent Chart

1.0 DESCRIPTION

The DP8 is a Synchronous Modem Interface which provides facilities for Modem Control, Parallel-to-Serial -- Serial-to-Parallel Data Conversion, Level Conversion, Character Detection and a program controlled Interface to the PDP8/E.

Data exchange between the PDP and the DP8 is accomplished via the Data Break facility and takes place in parallel while data between the DP8 and the Modem are in serial.

The Synchronous Modem Interface, as an assembly, consists of two quad modules (M839 and M866), and a cable terminated by a modem connector.

The DP8 Assembly may be programmed (by instruction and/or jumper selection) for Device Code, Character Detection, access address location, Character Length, Clock Phase, Data Break Priority, Carrier on and/or Off Detection, Sync Code, Data Field (to 32K) and for: current mode (as 301 and 303 Modems), Bi-polar (EIA/CCITT), and TTL level conversion. Additionally, there are provisions for accomodating an external clock.

2.0 SPECIFICATIONS

2.1 Modem interface: Designed to accomodate Bell 201, 301 and 303 Series Modems or equivalent. Jumper selection provides for current mode, Bi-polar or TTL Interface.

2.2 Transfer Mode: Full Duplex or Half Duplex*

2.3 Character Parameters:

2.3.1 Bits Per Character available are 6, 7, or 8.*

2.3.2 BAUD Rate: 71,000 BAUD (MAX. for 4 character recognition; 85,000 BAUD for 2 character recognition; and 100,000 BAUD for Ø char recognition).

2.4 Data Transfers: Transfers are maintained via three single cycle data breaks (1.4 micro seconds each cycle) for both transmit and receive. An additional cycle is required for each special character to be tested for (receive circuits only). Transfer to and from core is accomplished in any

*Jumper selectable.

field. The word Count, Current Address, and Characters for test (Character Recognition) is located in a specified location within field Zero.

2.5 Control Transfers: Control transfers are maintained via the Data Bus. The types of control available are: Idle, Terminal Ready, Enable, Transmit Request and Transfer Field.

2.6 Clocks: The clocks are normally provided for by the Modem. The exception is anticipated by providing split lugs for insertion of a local clock at the M866 Level Converter Module.

2.7 Device Codes: The M839 is programmable for one of four Instruction Sets. Each Instruction Set is composed of two device codes and is paired as follows:

640X/641X or 642X/643X or 644X/645X or 646X/647X or 650X/651X or 652X/653X or 654X/655X or 656X/657X.

2.8 Options: The only options are cable sets to service the 201, 301 and 303 Series Modems.

2.9 Cycle Time: Single Cycle Data Break -- 1.4 Micro Seconds
All Instructions -- 1.2 micro seconds.

2.10 Response Time

2.10.1 Data Transfers: 1/BAUD

2.10.2 Program Interrupt: One Character Time for Active Flags. (i.e. Word Count and character detected)

2.11 Break Priority: The M839 can be programmed (Jumper) for one of seven priorities. (1 through 7)

2.12 Character Recognition: The hardware will detect four (4) program selected characters. A Flag Bit, stored with the character, determines if the hardware will Flag the Program or strip the character upon detection.

2.13 Power Consumption

2.13.1 M839 +5 1.4 Amps
2.13.2 M866 +15 .05 Amps
-15 .105 Amps
+5 .4 Amps

2.14 Access Address: Access Address is selected by groups of 16 locations in field zero. The selection is made by jumpers and the first address of each group is confined to 7600, 7620, 7640, 7660, 7700 and 7720. The underlined will be standard for the DP8-EA,B, See Section 3.1.2 for current address, word count and character (detection) assignments within the 16 word groups.

2.15 Synchronizing Character:

Transmit: Non-hardware function - must be part of data for transmission.

Receive: The Receive Synchronizing Character (SYNC) is jumper selected. Two or more consecutive (SYNC) characters must be received before the hardware will be activated.

2.16 Modem Compatability (Typical)

Type	Speed Baud
Bell 201A	2000
201B	2400
205B	600; 1200; 1800 (with modification for fixed speed select)
301B	40,800
303B,C	19,000 to 50,000 (Synchronous only)
Rixon FM12	1200
Rixon Sebet 48	4800
GE TDM Series	2400
Lenkurt 26C	170-2400
etc.	

2.17 Carrier Detect: Jumper selection detects carrier/AGC ON and/or OFF transitions.

3.0 PROGRAMMING

3.1 Bit Assignments and/or Description

3.1.1 Status: The AC assignments are as follows: (Assertion = True)

3.1.1.1 Status 1 (SRS1)

AC00 R-RQST: Indicates a received character is ready for transfer to core.

AC01 T-RQST: Indicates a transmit request for data.

AC02 SYNC 2: The hardware synchronized on two incoming SYNC characters.

AC03 SYNC 1: The hardware synchronized on the first SYNC character. This bit will be maintained if two consecutive SYNC characters are detected.

AC04 RECEIVE Field EMA0

AC05 RECEIVE Field EMA1

AC06 RECEIVE Field EMA2

AC07 MODEM Ready: Indicates that either interlock or data set ready is ON.

3.1.1.2 Status 2 (SRS2)

AC00 Carrier/AGC: Indicates that either the carrier or the AGC is ON.

AC02 Terminal Ready

AC03 Clear to Send

AC04 Transmit Field EMA0

AC05 Transmit Field EMA1

AC06 Transmit Field EMA2

AC07 Receive Data (inverted)

3.1.2 Access Address

The access address is assigned (by jumpers) in even groups of 16 addresses. The hardware utilizes a four bit counter to select eight of the sixteen addresses for word count, current address and character recognition.

The following list, in binary, is the four low order bits, as they apply to the access addresses namely 7600, 7620, 7640, 7660, 7700 and 7720.

Receive cycles:

- 0000 Test Character
- 0001 Test Character

  (Starting access address for 4 character recognition.)
- 0010 Test Character
- 0011 Test Character

  (Starting access address for 2 character recognition.)
- 0100 Receive Word Count complimented
- 0101 Receive current address

Transmit cycles:

- 0111 Transmit word count complimented
- 1000 Transmit current address

- 0110
- 1001

*

1010
1011 Not Used
1100
1101
1110
1111

*Access address counter increments to these locations prior to character transfer with the PDP. When the counter is set at 0110, a Received Character has been transferred to a location specified by the Receive Current Address. When the counter is set at 1001, a character for transmit has been transferred to the DP8 from the location specified by the Transmit Current Address.

3.1.3 Word Count (WC) is a 12 bit right justified word used to count the number of words transmitted or received by the DP8. WC is the ONE's complement of the number of words desired to be transferred.

Example: $5_{(8)}$ Words to be Received or Transmitted

Quantity	000 000 000 101
Complement	111 111 111 010
Word Count	111 111 111 010

Current Address (CA) is a 12 bit right justified word used as a Memory Address for transferring data to or from core (receive or transmit) during Data Break functions. The Transfer Address is the CA+1. The first transfer will be from CA+1. The last transfer will be from CA + Number of Transmit.

Example: CA 111 000 111 111
Trans. Add 111 001 000 000 (CA+1)
Trans Address After $15_{(8)}$ Trans 111 001 001 101

NOTE: Current Address will always show either the last location data was transferred to/from or one less than the next address data will be transferred from/to.

3.1.4 Transmit and Receive Data: the 6,7, or 8 bit character is right justified. When 6 or 7 bit characters are used, the remaining bits up to 8 should be negated.

3.1.5 Control Word: The AC bits vs. Control are as follows:

AC00 Terminal Rdy
AC01 IDLE (1)
AC02 Enable (2)
AC03 Send ROST
AC04 For customer use (Write only TTL output)
AC05 For customer use (Write only TTL output)

1. If work count goes to zero while in IDLE mode, the Transmit Current address and Word Count will no longer be incremented and access to the last address will continue until the instruction SGTT (Ttransmit Go) is assigned or the IDLE Bit is negated.

2. If Enable is negated, Interrupt Request, Break in progress and Break Priority Gates are inhibited and the Break Request Flip Flop is latched in the ZERO state.

3.1.6 Character Recognition: Character recognition (detection) is accomplished for 6, 7, or 8 bit characters. The characters must be stored (see 3.1.2) right justified. When 6 or 7 bit characters are used, the remaining bits, up to 8, should be negated.

The stripping or flag generation upon character detection is dependent upon MD00. If MD00 is set to a ONE and the stored character is found to compare with the received character, further memory cycles will be terminated (i.e. the word count and current address will not be incremented and there will be no stored character). If MD00 is a ZERO and there is a character comparison, the character detected flag will be raised, the number of the recognized character will be stored for one character time in a two bit register, and the received character will be transferred to the current address +1.
Character Recognition is selectable for either 4 characters (locations zero through three) or 2 characters (locations two and three), Character recognition is also DE-SELECTABLE (no character recognition) allowing a higher speed limit by taking only 6 cycles for full duplex operation instead of 8 (with 2 char detection)or 10 (with 4 char detection) cycles.

3.1.7 Field Selection:

The selected field (increments of 4K of core up to 32K) combined with the current address forms a 15 bit address for transfers to and from core.

The field for character transfer is specified by program instruction (SLFL) and the contents of the AC. The field vs. AC assignments are as follows:

AC00
AC01 } Receive field (octal 0-7)
AC02

AC03
AC04 } Transmit field (octal 0-7)
AC05

3.1.8 Character Detected (Reading of)

When the instruction "Read Character Detected (SRCD)" is used to determine what character was detected, two bits, corresponding to the two low-order bits of the Access Address are transferred to AC10 and AC11 as follows:

AC10	AC11	Access Address (Base 2)
0	0	0000
0	1	0001
1	0	0010
1	1	0011

3.2 Instructions

3.2.1 Detailed

NOTE: All instructions are fully decoded and two device codes are required for an instruction set. Up to eight sets of instructions are available and are paired as follows:
640X/641X, 642X/643X, 644X/645X, 646X/647X.
650X/651X, 652X/653X, 654X/655X, 656X/657X.

INSTRUCTION	DESCRIPTION
Transmit Go (SGTT) 6405/6425 6445/6465 6505/6525 6545/6565	SGTT sets the Transmit Go Flip Flop. This instruction implies that the program is ready to transmit data (i.e. the Current Address (CA) and Word Count (WC), have been updated). Upon receipt of this instruction, provided Clear to Send (CS) has been received in response to Request to Send (RS), memory references will begin immediately. Memory references will cease only when Word Count (WC) decrements to zero (WC → Ø). In this event if SGTT is not issued in one character time, the transmit line will be maintained at mark hold. Transmit Request should be asserted (SLCC instruction) and should not be cleared until two bit times after the last bit has been transmitted or 1/Baud x (bits per character +2) seconds after overflow.
Receive Go (SGRR) 6404/6424 6444/6464 6504/6564 6544/6564	SGRR sets the Receive Go Flip Flop. This instruction implies that the program is ready to receive data from the communications line, (i.e. the Current Address (CA) and Word Count (WC,)) have been updated. The hardware, upon receipt of this instruction, will begin memory references if two consecutive synchronizing characters have been recognized by the hardware on the incoming serial data line. Memory references will cease only when WC decrements to Zero (WC → Ø) and SGRR is not issued in less than one character time.
Skip if Character Detected (SSCD) 6400/6420 6440/6460 6500/6520 6540/6560	The SSCD Instruction causes the program to skip the next instruction if the character detect flag is a ONE. The character detect flag is a ONE if an assembled character is found to compare one of the stored characters in one of the first four locations of the Access Address. Additionally, the SSCD Instruction clears the character detected flag. If the program is required to identify which of the four stored characters compared to the contents of the Receive Buffer, then a Read Character detected (SRCD Instruction should be utilized. See the SRCD instruction for details).

INSTRUCTION	DESCRIPTION
Clear Sync Detect (SCSD) 6506/6406/6426/6526 6546/6446/6466/6566	Clears the "Sync Character Detection" Flip Flops. This instruction enables the programmer to initialize the sync detection circuits and clear the receive registers without initializing the modem interface.
Skip if Receive Word Count O'Flow (SSRO) 6502/6402/6422/6522 6542/6442/6462/6562	Skips the next instruction and clears the flag if the Receive O'Flow Flag is a ONE. The Receive O'Flow Flag is a ONE if during the Receive Data break sequence the Word Count (in core) overflowed.
Clear Synchronous Interface (SCSI) 6501/6401/6421/6521 6541/6441/6461/6561	Initializes all active functions in the synchronous interface.
Read Transfer Addr. Register 6407/6427 6447/6467 6507/6527 6547/6567	Transfers the contents of the Transfer Address Register to AC00-AC11. In use, the Transfer Address Register latches the Current Address+1 (CA+1) prior to returning it to core. During Data Transfers (Transmit or Receive) this register then becomes the 8/E's Memory Address (MA). This instruction is primarily for diagnostic and/or program debug.
Load Control (SLCC) 6412/6432 6452/6472 6512/6532 6552/6572	Transfers the contents of AC00-AC05 for selecting Terminal Ready, Idle Mode, Synchronous Interface Enable, Transmit Request, and selectable functions respectively. (AC00) Terminal Ready permits the modem to enter into the data mode.

	(AC01) Idle Mode allows a continuous transmission from the same location in core without program intervention. The hardware will enter the Idle Mode when the Word Count goes to ZERO. Further, the transmit current address and Word Count will no longer be incremented and access to the last address will continue until the SGTT Instruction is issued or the Idle Bit is negated. (AC02) Interface Enable allows program interrupts and data break cycles. (AC03) Transmit Request activates the Request to Send line. See SGTT instruction. (AC04, AC05) are for customer use. When modem timing signals are used, one EIA (or current mode) transmitter is available to be used with AC04 or AC05.
Skip if Ring Flag (SSRG) 6410/6430 6450/6470 6510/6530 6550/6570	Skips the next instruction and clears the Ring Flag if the Ring Flag is a ONE.

Skip if Carrier AGC Flag (SSCA)

6511/6411/6431/6531
6551/6451/6471/6571

Skips the next instruction and clears the Carrier/AGC Flag if the Flag is in the ONE state. The Carrier/AGC Flag is in the ONE state if the Carrier/AGC line has made an ON and/or OFF transition. The detected transitions are jumper selectable.

Read Status 2 (SRS2)

6414/6434
6454/6474
6514/6534
6554/6574

Transfers status to AC00-AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. Status is as follows:

AC00	Carrier/AGC	
AC01	Request to Send	
AC02	Terminal Ready	
AC03	Clear to Send	
AC04	TEMA 0	} Field Select Register
AC05	TEMA 1	
AC06	TEMA 2	
AC07	Receive Data (inv.)	

Read Status 1 (SRS1)

6415/6435
6455/6475
6515/6535
6555/6575

Transfers status to AC00-AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. Status is as follows:

AC00	R-RQST	Receive and Transmit
AC01	T-RQST	Break Requests
AC02	Sync 2	Received "Sync"
AC03	Sync 1	Characters
AC04	REMA 0	} Field Select Register
AC05	REMA 1	
AC06	REMA 2	
AC07	Modem Ready	

Load Field (SLFL)

6413/6433
6453/6473
6513/6533
6553/6573

Transfers the contents of AC00-AC05 to the field select registers. AC03-AC05 selects the transmit field while AC00-AC02 selects the Receive Field. The selected field (increments of 4K of core -- up to 32K) combined with the current address forms a 15 bit address for data transfers to and from core.

Skip if Transmit Word Count O'Flow (SSTO)

6503/6403/6423/6523
6543/6443/6463/6563

Skips the next instruction and clears the flag if the Transmit O'Flow Flag is a ONE. The Transmit O'Flow Flag is a ONE if during the Transmit Data Break sequence the Word Count (in core) overflowed.

Skip on Bus Error (SSBE)

6416/6436
6456/6476
6516/6536
6556/6576

Skips the next instruction and clears the Bus Error Flag if the flag was in the ONE state. The Bus Error Flag will be in the One state if a Transmit or Receive Break Request has not been serviced in less than 1/BAUD time. This flag implies that the Break bus is either overloaded or is inoperative.

Read Character Detected (SRCD)

6417/6437
6457/6477
6517/6537
6557/6577

The contents of a two bit register which contains the address of the detected character is transferred to AC10 and AC11. The two bits correspond to the two low order bits of the access address where the characters for detection are stored.

Maintenance Instruction

The SRCD instruction issued when AC00 is set to a ONE causes a single clock pulse on the Maintenance Clock line to the modem. In the test configuration (Figure 1) this line is returned as the transmit and receive clocks enabling single step testing of the transmit and receive circuits.

3.2.2 Summary of Instructions
(FOR ADDITIONAL IOT CODES READ 65XX INSTEAD OF 64XX)

CODE	MNEMONIC	INSTRUCTION
6400/6420/6440/6460	SSCD	Skip if character detected
6401/6421/6441/6461	SCSI	Clear Synchronous Interface
6402/6422/6442/6462	SSRO	Skip if Receive Word Count O'Flow
6403/6423/6443/6463	SSTO	Skip if Transmit Word Count O'Flow
6404/6424/6444/6464	SGRR	Receive Go
6405/6425/6445/6465	SGTT	Transmit Go
6406/6426/6446/6466	SCSD	Clear Sync Detect
6407/6427/6447/6467	SRTA	Read Transfer Address Register
6410/6430/6450/6470	SSRG	Skip if Ring Flag
6411/6431/6451/6471	SSCA	Skip if Carrier/AGC Flag
6412/6432/6452/6472	SLCC	Load Control
6413/6433/6453/6473	SLFL	Load Field
6414/6434/6454/6474	SRS2	Read Status 2
		AC00 Carrier/AGC
		AC01 Request to Send
		AC02 Terminal Ready
		AC03 Clear to Send
		AC04 TEMA 0
		AC05 TEMA 1
		AC06 TEMA 2
		AC07 Receive Data (Inv.)
6415/6435/6455/6475	SRS1	Read Status 1
		AC00 R-RQST
		AC01 T-RQST
		AC02 SYNC 2
		AC03 SYNC 1
		AC04 REMA 0
		AC05 REMA 1
		AC06 REMA 2
		AC07 Modem Ready
6416/6436/6456/6476	SSBE	Skip on Bus Error
6417/6437/6457/6477	SRCD	Read Character Detected Low Order Bits (Access Address) AC10 and AC11
6417/6437/6457/6477 with AC00 - ONE	----	Maintenance Clock

4.0 MISCELLANEOUS

4.1 Test Procedure

Test Connector DEC Part # 70-08372 wired as shown in Figure 4.1 coupled with the instruction SRCD issued with AC00 = ONE (maintenance clock) is used to exercise and/or test the DP8-EA,B,

The DP8-EA,B diagnostic is MAINDEC 08-DHDPA.

NOTE: THE FOLLOWING MIST BE FOLLOWED IN ORDER TO INSURE PROPER DIAGNOSTIC FUNCTIONING

CLOCK PHASE JUMPERS FOR THE RECEIVE CLOCK MUST BE INSERTED ACCORDING TO THE FOLLOWING TABLE

MODE	PHASE	NORMAL	INVERTED
*ON-LINE	NORMAL	IN	OUT
**OFFLINE	INVERTED	OUT	IN
CUSTOMER	((AS SPECIFIED BY THE CUSTOMER))***		

CLOCK PHASE JUMPERS FOR THE TRANSMIT CLOCK WILL INSERTED ACCORDING TO THE FOLLOWING TABLE

MODE	PHASE	NORMAL	INVERTED
*ON-LINE	NORMAL	IN	OUT
**OFFLINE	NORMAL	IN	OUT
CUSTOMER	(((AS SPECIFIED BY THE CUSTOMER))***		

*Normal Bell 201 Modem configuration.
**Diagnostic program configuration.
***There are instances when the customer may desire a different than standard clock phase scheme, and may so specify.

DP8-E Interface	I/O Conn.	Cable Terminating Connector EA/EB DB25P	Test Connector EA/EB* DB25S Pins
Send Request	V	4	4
Clear to Send	T	5	5
Interlock/Data Set Ready	Z	6	6
Send Data	F	2	2
Received Data	J	3	3
Maintenance Clock	FF	11	11
Serial Clock Receive	R	17	17
Serial Clock Transmit	N	15	15
Terminal Ready	DD	20	20
Carrier/AGC	BB	8	8
Ring	X	22	22
Frame Ground	UU	1	1
Signal Ground	VV	7	7
#For Customer Use	FF	11	
	JJ	12	

*EB test connector and cable are tested the same as above.
The pinning and test connector designation are different.
#TTL Output Jumper Selectable to External Clock Transmitter for EIA Output

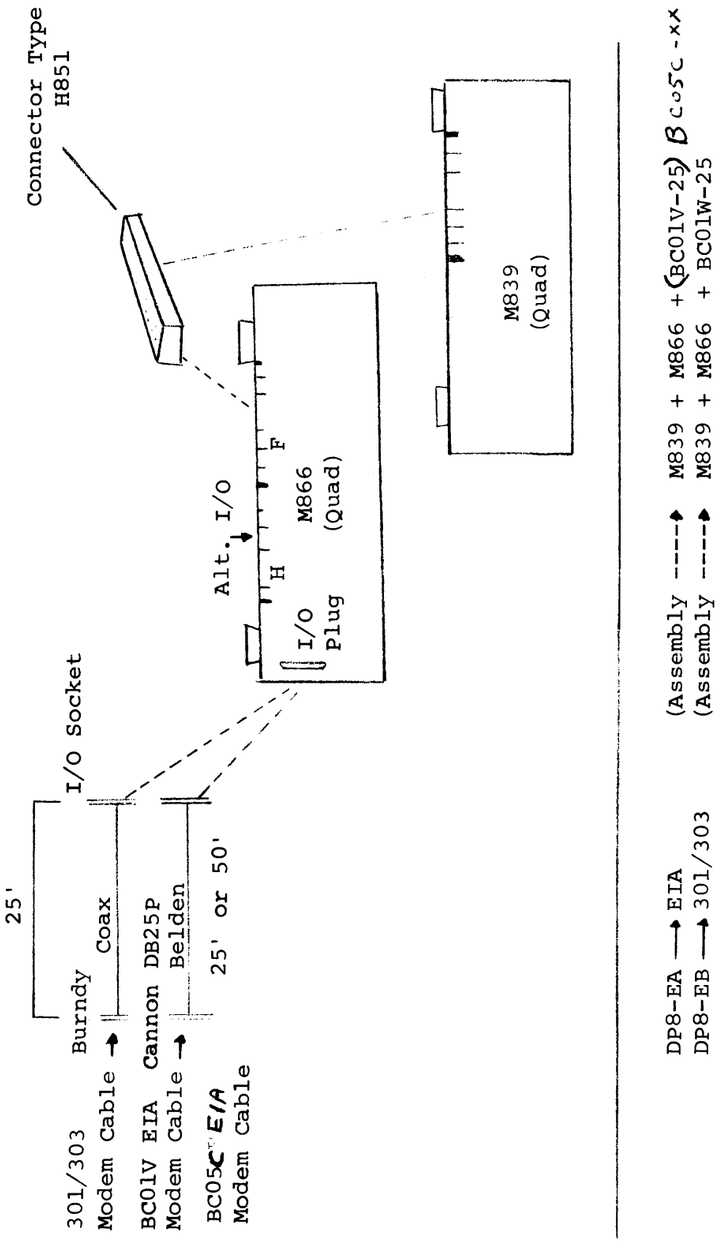
TEST CONNECTOR
Figure 4-1

4.2 DP8-E Terminated Modem Leads

The following chart shows the modem control leads for models 201, 301 and 303 as used in the DP8-E. Unless otherwise specified the 201 levels are Bi-polar levels while the 301 and 303 are current mode.

Logic Print	Model 301 (EB)	Model 303 (EB)	Model 201 (EA)
Send Data	Send Data	Send Data	Send Data
Received Data	Received Data	Receive Data	Receive Data
Clear to Send	Clear to Send	Clear to Send	Clear to Send
Interlock/Data Set Ready	Interlock	Data Set Ready	Interlock
Carrier/AGC	Carrier On-Off	AGC Lock	Carrier on-off
Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit
Serial Clock Receive	Serial Clock Receive	Serial Clock Receive	Serial Clock Receive
Terminal Ready		Data Terminal Rdy*	Remote Control
Ring		Ring Indicator*	Ring Indicator 1
External Timing	Serial Clock Transmit (External)	Serial Clock Transmit (External)	External Timing
Request to Send	Send Request	Send Request	Send Request

*Bipolar



4.4 The DP8-EA/EB modules (M839 and 866) are equipped with a number of jumpers to allow maximum freedom in configuration.

M839 Jumpers:

A. Device codes are selectable with the jumpers labeled 5, N5, 6, 7, N6, and N7.

B. The number of bits per character is selected with the jumpers labeled B9, B8, B78, B7, B6, C8, and C7.

C. The Access Address is selected with the jumpers labeled A5,A6, and A7.

D. The Break Request priority is selected by jumpers P1,P2,P3,P4,P5,P6, and P7.

E. The Sync code is selected by jumpers labeled S4,S5,S6,S7,S8,S9,S10 and S11.

F. Character Recognition locations are selected with jumpers 2 and 4.

M866 Jumpers:

A. The clock Phase is selected by the two or two N jumpers.

B. The Carrier AGC Transition is selected by the ON and OFF jumpers.

C. Break Priority Detection is selected by the jumpers labeled P1,P2,P3,P4,P5,P6,P7.

D. The Level Conversion selection is provided by the jumpers labeled T, CT, CE, E and C.

E. External Timing Output is provided by jumper L.

F. External Timing for diagnostic purposes suing EIA pin 11 is provided by jumper F.

G. Jumpers X and D provide signals necessary for auto answering with the Bell 303 modem.

H. An internal clock is available with jumper ICL. (With cap it is set to 45000 BAUD) T =.87 (C)(220).

4.4.1 Jumper Selection Guide

Unless otherwise specified, the following selections will be made by Production:

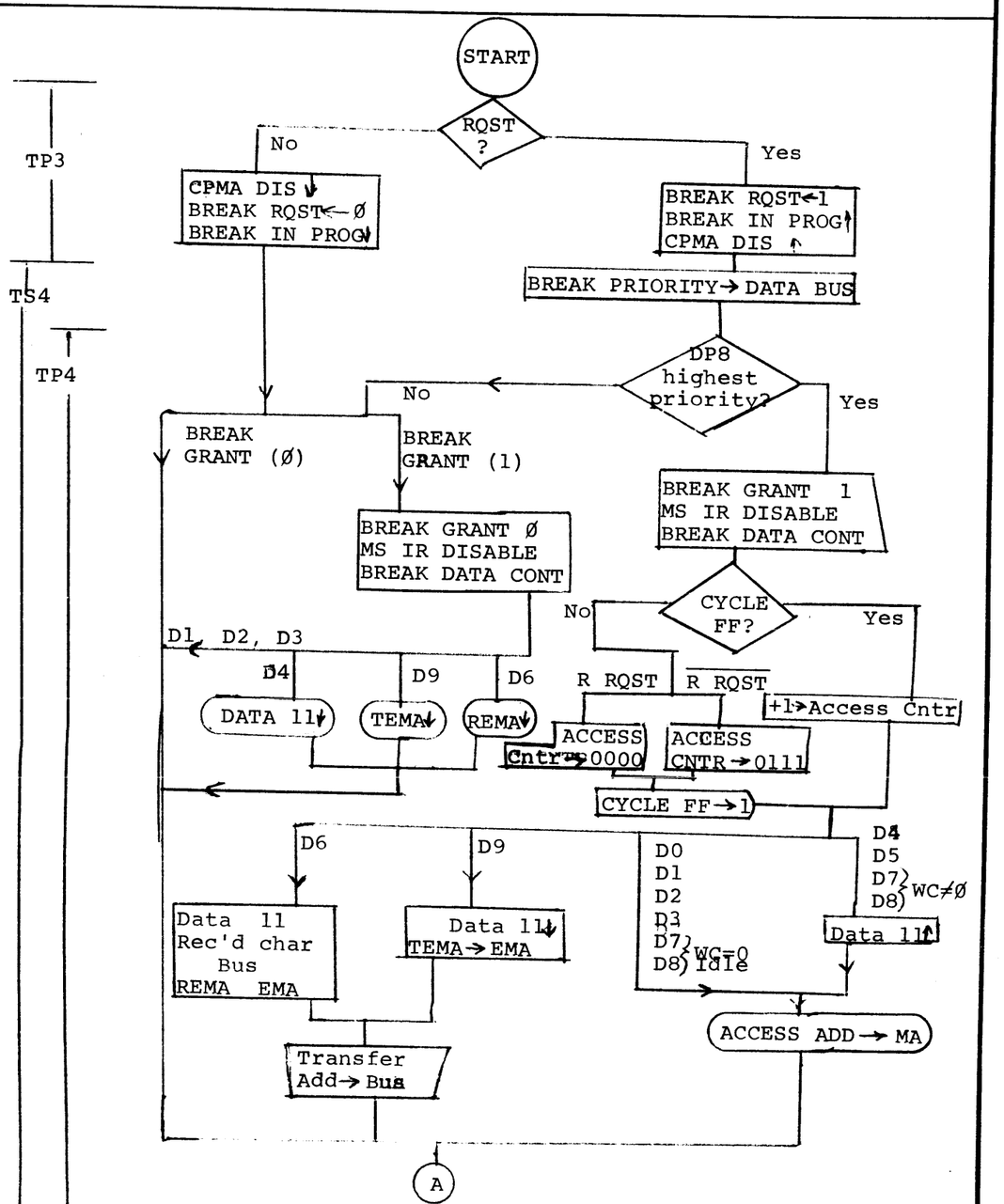
a.

DP8-E A,B	ACCESS ADDRESS	IOT CODES	BREAK PRIORITY
1st	7720-7730	640X/641X	5
2nd	7700-7710	642X/643X	4
3rd	7660-7670	644X/645X	3
4th	7640-7650	646X/647X	2

b. 8 Bits/Character
c. Normal Clock Phase
d. Level conversion for DP8-EA will be EIA
e. Level conversion for DP8-EB, will be current mode.
f. Sync code will be 226 (Octal)
g. Carrier on/off transistions
h. Full Duplex

4.4.2 M839 Jumpers

	Select	Remove Jumper
Bits/Character	6	B8,B7,B78,C7,B9,
	7	B8,B6,C8,B9
	8	B7,B6,
Break Priority (Generate)	1	P2,P3,P4,P5,P6,P7
	2	P1,P3,P4,P5,P6,P7
	3	P1,P2,P4,P5,P6,P7
	4	P1,P2,P3,P5,P6,P7
	5	P1,P2,P3,P4,P6,P7
	6	P1,P2,P3,P4,P5,P7
	7	P1,P2,P3,P4,P5,P6
Access Address	7720(1)	A6
	7700(2)	A6,A7
	7660(3)	A5
	7640(4)	A5,A7
	7620(5)	A5,A6
	7600(6)	A5,A6,A7
Device Code (see pg. 28 note 2)	640X/641X(1)	5,6,7
	642X/643X(2)	5,6,N7
	644X/645X(3)	5,N6,7
	646X/647X(4)	5,N6,N7
Sync Code	226	S5,S6,S8,S11
Character Recognition Locations	0	2 (SEE NOTE 3)
	2	4
	4	NEITHER



NOTES: (1) 1st DP8 (2) 2nd DP8 (3) 3rd DP8
(4) 4th DP8 (5) Spare

4.4.3 M866 Jumpers*

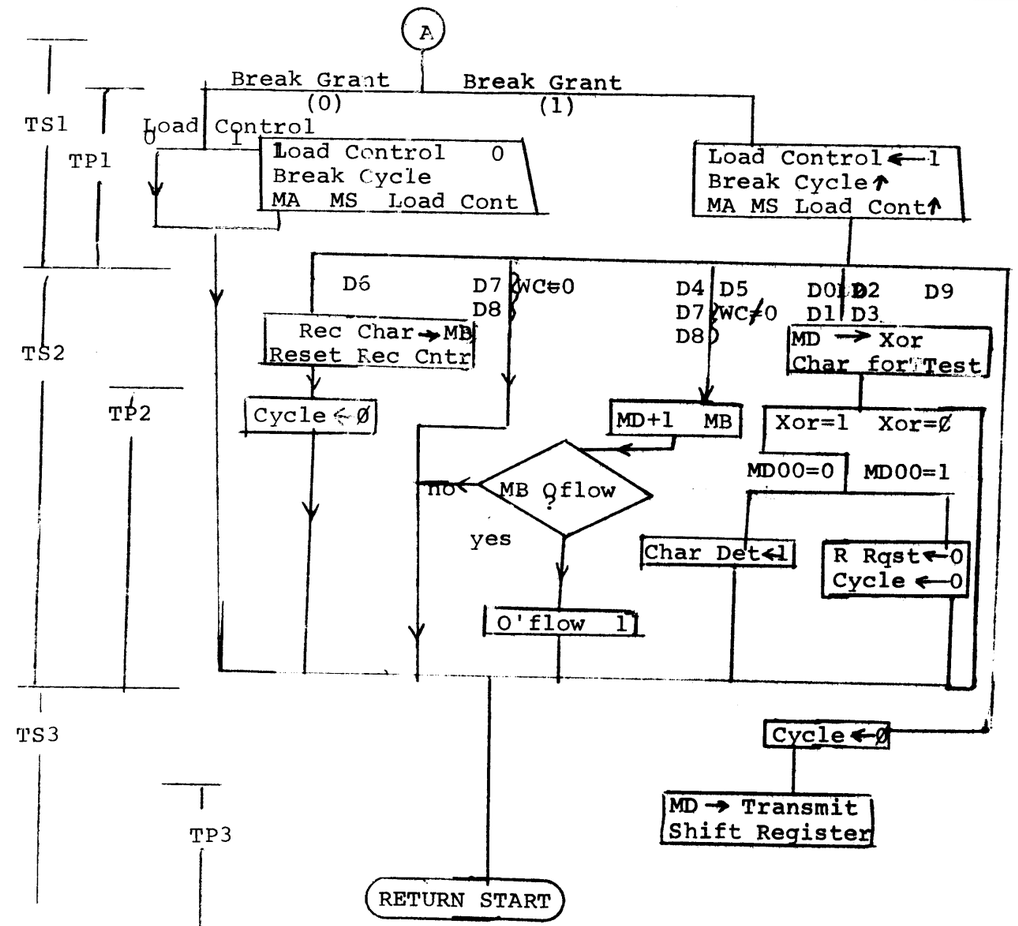
*Jumpers are production inserted with the exception of: C and △, FF, JJ, L

	Select	Remove Jumper	Add Jumper
CO/AGC Transition	ON	OFF	
	OFF	ON	
	ON & OFF		ON+OFF
***Clock Phase	Inverted	N(TWO)	△(TWO)
Level Conversion	EIA	T,CT	
	Current	T,E	C(Six)
	TTL	E,CE	
Break Priority (Detect)	1	P1 - P6	
	2	P2 - P6	
	3	P3 - P6	
	4	P4 - P6	
	5	P5 - P6	
	6	P6	
	7	-------	
Diagnostic Test	Test	N (recv)	△ (Recv)
Full Duplex		HD	
Modem timing		ICL, L	
Bell 300 series	301	X, D	
	303		X, D

*** For proper diagnostic operation the following clock jumper configuration is required:

CLOCK PHASE	TRANSMIT	RECEIVE	SYMBOL
NORMAL	XXXX		N
INVERTED		XXXX	Δ

The jumpers changed to run the diagnostic program should be changed back to conform to the customers configuration (i.e. the usual configuration when using Bell modems is transmit and receive clocks both normal clock phase).



1. D0-D9 refer to the addresses selected by the access address.
2. Symbol meaning
   ↑ = assertion
   ↓ = nonassertation (cleared)
   ⇄ = goes to

4.6 Top Connector and I/O Pin Assignments

M839 M866 "F" Connector

Name	Source M839	Source M866	Pin
SRCD (Low)		*	FA1
This Code (Inverted)	*		FB1
INT RQST	*		FC1
REC DATA (Mark +3)		*	FD1
REMA (Inverted)	*		FE1
TEMA (Inverted)	*		FF1
SCR-P (Inverted)		*	FH1
BREAK GRANT		*	FJ1
INITIALIZE (Inverted)	*		FK1
GTP4		*	FL1
BREAK RQST		*	FM1
SSBE (Inverted)		*	FN1
SCRT (Inverted)		*	FP1
CS		*	FR1
SD	*		FS1
IDLE		*	FT1
RQST	*		FU1
SRS1	*		FV1
Ground			FB2-V2
Spare			None
CNTL			FA2

I/O CONNECTORS

Name	Edge	"H"	EIA	301	303
Signal Ground	VV	HC2	7	All Shields	(ALL) (NOTE 1)
Frame Ground	B	HT1	1		
Clear to Send	T	HK2	5	C	C
Receive Data	J	HF2	3	K	K
Interlock/Data Set Ready	Z	HN2	6	F	F
Serial Clock XMIT	N	HH2	15	J	J
Serial Clock Receive	R	HJ2	17	L	L
Carrier/AGC	BB	HP2	8	M	M
Ring	X	HM2	22	-	F(OUTER)
Send Data	F	HE2	2	E	E
Terminal Ready	DD	HR2	20	-	M(OUTER)
Send Request	V	HL2	4	D	D
External Timing (EIA OUTPUT)	L	HH1	24	H	H
-6 Volts	-	HC1	-	-	-
+6.4 Volts	-	HS2	-	-	-
External Clock (TTL INPUT)	L	HV2	-	-	-
SEC Transmit Data	FF	-	-	-	-
SEC Receive Data	JJ	-	-	-	-

NOTE 1: 303 Modem connectors F + M shields (outer connector) carry EIA signals as indicated.

NOTE 2: To allow greater flexibility IOT sets 65XX may be selected instead of/ in addition to 64XX IOT sets through the use of the 5 or N5 jumpers.

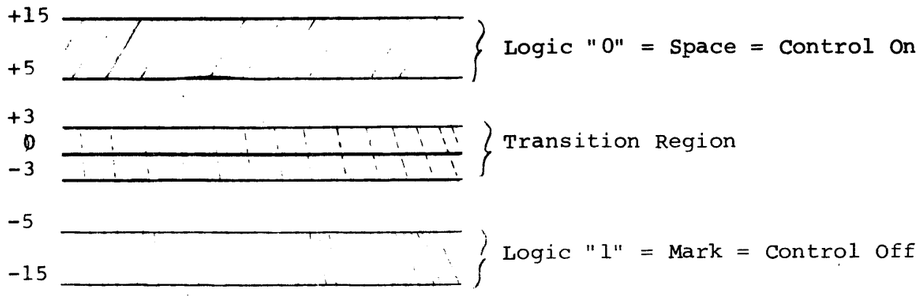
IOT SELECTED	JUMPER INSTALLED	CONFIGURATION REMOVED
650X-651X	5,N6,N7	N5,6,7
652X-653X	5,N6,7	N5,6,N7
654X-655X	5,6,N7	N5,N6,7
656X-657X	5,6,7	N5,N6,N7

NOTE 3: Remove S (number) to select A zero for that Bit .

APPENDIX "A"

RS-232-C Electrical Specifications

Driver output logic levels with 3K to 7K load	15 volts > V_{oh} > 5V -5 volts > V_{ol} > -15V
Driver output voltage with open circuit	V_o < 25 volts
Driver output impedance with power off	Z_o > 300 ohms
Output short circuit current	I_o < 5 amps
Driver slew rate	$\frac{dv}{dt}$ < 30 volts/usec.
Receiver input impedance	7K ohms > R_{in} > 3K ohms
Receiver input voltage	±15V compatible w/driver
Receiver output with open circuit input	Mark
Receiver output with 300 ohms to ground on input	Mark
Receiver output with +3 volt input	Space
Receiver output with -3 volt input	Mark



APPENDIX B

Current Mode Electrical Specifications (Applicable to the Bell 300 Series Modem or equivalent

Receiver Input Current/Voltage levels with 100 ohms Termination
Mark 5 ma (-0.7< Ein< 1)

Driver Output Impedance with Power Off:
Not Specified

Driver Output Short Circuit Current
Not Specified

Driver Slew Rate between the 7 ma and the 21 ma levels
Typical 14 ma/100 ns
Max. 14 ma/ 50 ns
Min. 14 ma/200 ns

Receiver Input Impedance
120 > Zin > 90

Receiver Output with Open Circuit Input
Logic one - Mark-off

Receiver Output with Input > 23 ma
Logic Zero - Space - On

Receiver Output with Input < 5 ma
Logic ONE - Mark-off

Driver Distortion Limits
Mark to Space or Space to Mark must be achieved within 25% of bit interval.

Receiver Open Circuit Voltage
-0.8 to -1.3

APPENDIX C

Pin Number	Circuit	Description
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground (Common Return)
8	CF	Received Line Signal Detector
9	--	(Reserved for Data Set Testing)
10	--	(Reserved for Data Set Testing)
11	--	Unassigned
12	SCF	Sec. Rec'd Line Sig. Detector
13	SCB	Sec. Clear to Send
14	SBA	Secondary Transmitted Data
15	DB	Transm. Signal Element Timing (DCE Source)
16	SBB	Secondary Received Data
17	DD	Received Signal Element Timing (DCE Source)
18		Unassigned
19	SCA	Secondary Request to Send
20	CD	Data Terminal Ready
21	CG	Signal Quality Detector
22	CE	Ring Indicator
23	CH/CI	Data Signal Rate Selector (DTE/DCE Source)
24	DA	Transmit Signal Element Timing (DTE/DCE Source)
25		Unassigned

EIA RS-232-C Interface Pin Assignments

APPENDIX D

Inter-Change Circuit	CCITT Equivalent	Description
AA	101	Protective Ground
AB	102	Signal Ground/Common Return
BA	103	Transmitted Data
BB	104	Received Data
CA	105	Request to Send
CB	106	Clear to Send
CC	107	Data Set Ready
CD	108.2	Data Terminal Ready
CE	125	Ring Indicator
CF	109	Received Line Signal Detector
CG	110	Signal Quality Detector
CH	111	Data Signal Rate Selector (DTE)
CI	112	Data Signal Rate Selector (DCE)
DA	113	Transmitter Signal Element Timing (DTE)
DB	114	Transmitter Signal Element Timing (DCE)
DD	115	Receiver Signal Element Timing (DCE)
SBA	118	Secondary Transmitted Data
SBB	119	Secondary Received Data
SCA	120	Secondary Request to Send
SCB	121	Secondary Clear to Send
SCF	122	Sec. Rec'd Line Signal Detector

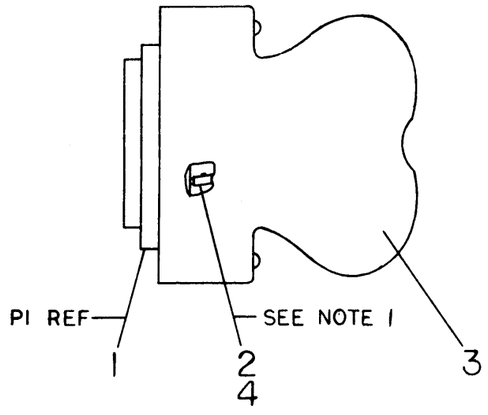
EIA (RS-232-C) to Equivalent CCITT

WIRE TABLE

ITEM NO	DESCRIPTION AWG	COLOR	CONNECTION FROM	TO	REMARKS
4	24	BLK	PI-4	PI-5	
			5	6	
			2	3	
			11	17	
			17	15	
			20	22	
4	24	BLK	PI-22	PI-8	

NOTES:

1 EACH SOLDERED CONNECTION ON P1 SHALL BE INSULATED WITH A 1/4 INCH PIECE OF HY-SHINK TUBING (ITEM NO. 2)



QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		
A/R	WIRE SOLID #24 BLACK	9107470-2	4
1	CANNON CONN. HOOD DB51226-1	12-05885	3
A/R	#14 WHITE ASTRA SUFLEX HIGH SHRINK TUBING	9107255	2
1	CANNON CONN. FEMALE DB-25S	12-04975	1

FIRST USED ON OPTION/MODEL: PDP11

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL //

FINISH //

DRN.	V. Bissonnette	DATE 3-5-71
CHK'D.	A. Raimondi	DATE 3-22-71
ENG.	R. Grace	DATE 3-25-71
PROJ. ENG.	R. Grace	DATE 3-25-71
PROD.	[signature]	DATE 3-26-71

NEXT HIGHER ASS'Y: A-PL-DP11-D-Ø

SCALE: NONE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
DP11-DA
TEST CONNECTOR

SIZE	CODE	NUMBER	REV
C	IA	7008372-0-0	

DIST. C

REVISIONS: REV. | CHANGE NO. | CHK.

DRAWING NUMBER: C IA 7008372-0-0 REV.

DEC FORM NO. D16 1265

WIRE TABLE

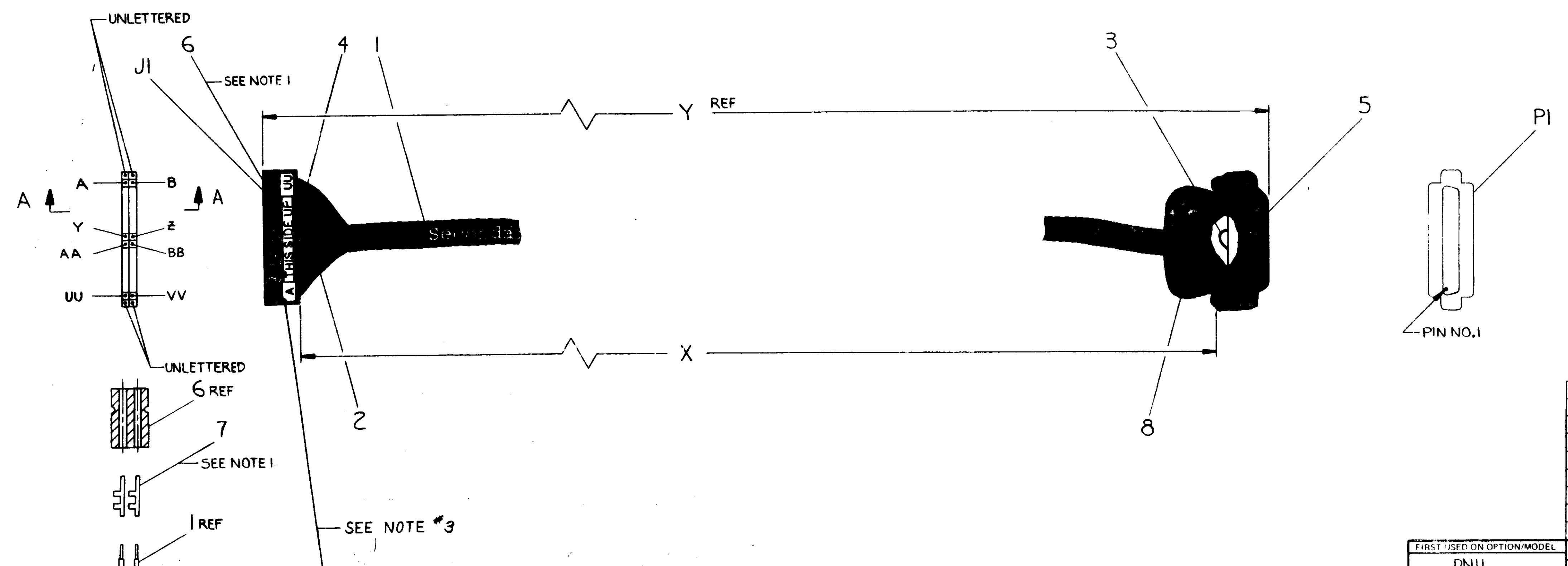
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
	22	BLU/WHT	P1-1		J1-VV	
		WHT/BLU	P1-2		J1-F	
		ORN/WHT	P1-3		J1-J	
		WHT/ORN	P1-4		J1-V	
		GRN/WHT	P1-5		J1-T	
		WHT/GRN	P1-6		J1-Z	
		BRN/WHT	P1-7		J1-UU	
		WHT/BRN	P1-8		J1-BB	
		SLA/WHT	P1-9		J1-Y	
		WHT/SLA	P1-10		J1-W	
		BLU/RED	P1-11		J1-FF	
		RED/BLU	P1-12		J1-JJ	
		ORN/RED	P1-13		J1-D	
		SLA/RED	P1-14		J1-LL	
1	22	SLA/GRN	P1-15		J1-N	
1	22	RED/BRN	P1-16		J1-NN	
		SLA	P1-17		J1-R	
		RED/SLA	P1-18		J1-U	
		BLU/BLK	P1-19		J1-P	
		BLK/BLU	P1-20		J1-DD	
		ORN/BLK	P1-21		J1-MM	
		BLK/ORN	P1-22		J1-X	
		GRN/BLK	P1-23		J1-RR	
		BRN/RED	P1-24		J1-L	
		RED/ORN	P1-25		J1-C	
		BLK	P1-1	4	J1-A	
1	22	BLK	P1-7	4	J1-B	
3	26	BLK	P1-1		P1-7	
2	26	RED	J1-E		J1-M	

LEGEND

NUMBER	VARIATION DIM X	VARIATION DIM Y (PRECUT)
BC05C-25	25'±3"	25'±6"
BC05C-50	50'±2%	50'±1.8"

NOTES:

1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
2. ONLY DEC PART # 1210090-0-0 MAY BE USED AS J1.
3. PLACE ITEM # 9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM # 6 (BERG HOUSING) AS SHOWN.



SECTION A-A

PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	3611567	9
1	HOOD, #DB51226-1 CINCH	1205885	8
29	SOCKET, #HT-68	1210089-5	7
1	HOUSING, #20383 BERG	1210090-0-0	6
1	PLUG, #DB-25P CINCH	1205886	5
A/R	TUBING, #22 AWG TEF BLK	9107256-00	4
A/R	WIRE, #26 AWG STRD TEF BLK	9107636-00	3
A/R	WIRE, #26 AWG STRD TEF RED	9107636-22	2
A/R	CABLE, 25 CONDUCTOR	9107736	1

FIRST USED ON OPTION/MODEL: DN11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX ±.005, XX ±.02
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL: —
FINISH: —

DRN. S. Roberts	DATE 11/3/71	
CHK. R. Cook	DATE 11/5/71	
ENG. [signature]	DATE 11/5/71	
PROJ. ENG. [signature]	DATE 11/5/71	
PROD. [signature]	DATE 11/9/71	

NEXT HIGHER ASSY.: —
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION, MAYNARD MASSACHUSETTS

TITLE: CABLE, MODEM BC05C

SIZE	CODE	NUMBER	REV.
D	UA	BC05C-0-0	B

REVISIONS

CHK	CHANGE NO.	REV.			
[signature]	BC05C-00001	A	[signature]	SMITH	7-14-72
[signature]	BC05C-00002	B	E. Allen	B. REGAN	10-29-73

DEC FORM NO DRD 100-A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY R. Allen DATE 2/15/72	CHECKED R H Smith DATE 2-17-72	SECTION
ENG R. Allen DATE 2-17-72	PROD R. K. Allen DATE 2-16-72	ISSUED SECT.

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY DP8-EA	QUANTITY DP8-EB
1	E-CS-M839-0-1	Synchronous Modem Interface	1	1
2	E-CS-M866-0-1	Synchronous Modem Interface	1	1
3	D-UA-BC05C-25-0	BC05C Cable Assy	1	-
4	D-UA-BC01W-25-0	BC01W Cable Assy	-	1
5	B-UA-H851-0-0	H851 Edge Connector	1	1
6	C-IA-700-8372-0-0	Test Connector	1	-

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DP8-E PARTS LIST	SHEET OF	A	PL	DP8-E-0		
		DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY R. Allen DATE 2/15/72	CHECKED RMS DATE 2-17-72	SECTION
ENG R.M. DATE 2-17-72	PROD K.A. DATE 2-16-72	ISSUED ECCT.

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DP8-EA	DP8-EB	KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	M839	Modem Interface	1	1		
2	M866	Modem Interface	1	1		
3	H851	Edge Connector	1	1		
4	BC05C-25	Cable	1	-		
5	BC01W-25	Cable	-	1		
6	7008372	Test Connector	1	-		
7*	DEC-8E-HR2B-D-DP8-EA/EB	Maintenance Manual (Prel)	1	1		
8	Maindec-8E-D8BA-D	Synchronous Modem Interface Diagnostic	1	1		

* If manual not available, ship Eng. Spec instead.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DP8-E Accessory List	SHEET OF	A	AL	DP8-E-4		
		DIST				